

Life cycle of an Embedded IC

from concept to end user

Dhanunjay Nalla
IC Staff Test Engineer

The image shows a Zoom meeting interface. On the left, there is a list of external contacts with their names and initials. On the right, a presentation slide is displayed with the title 'Recapitulation' in red. The slide contains four bullet points, each preceded by a right-pointing arrowhead. The first bullet point is 'What is an IC?' followed by a sub-bullet 'Integrate several circuits on a single substrate'. The second bullet point is 'What is the need of an IC?' followed by a sub-bullet 'To save space on devices/gadgets. PC vs Tablet vs Smart phone'. The third bullet point is 'What is an Embedded IC?' followed by a sub-bullet 'Make the device ready to use. IC -> device -> FW -> OS -> Apps'. The fourth bullet point is 'What is the importance of an Embedded IC?' followed by a sub-bullet 'Growing needs of the human being to become ...'.

Zoom

Home Chat Meetings Contacts Apps

Contacts Channels

Khushi Thakkar EXTERNAL
Mahiraj Parmar EXTERNAL
Manashvi Singh EXTERNAL
Manjit Kaur EXTERNAL
Mrigank Sharma EXTERNAL
Nagendra Verma EXTERNAL
Noel D EXTERNAL
Paramita Das EXTERNAL
Parth Bhatia EXTERNAL
parth sheoran EXTERNAL
raghav gupta EXTERNAL
Rahul Jagtap EXTERNAL
Rahul Singh EXTERNAL
Sahil Rihani EXTERNAL
Sanskar Syal EXTERNAL
Saqlain Momin EXTERNAL
Sarthak Patil EXTERNAL
Shivani Goyal EXTERNAL

Recapitulation

- What is an IC?
 - Integrate several circuits on a single substrate
- What is the need of an IC?
 - To save space on devices/gadgets. PC vs Tablet vs Smart phone
- What is an Embedded IC?
 - Make the device ready to use. IC -> device -> FW -> OS -> Apps
- What is the importance of an Embedded IC?
 - Growing needs of the human being to become ...



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Contacts

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- Sreya Vemuri EXTERNAL
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- Tapendra Rathore EXTERNAL
- Vaibhav Agrawal EXTERNAL
- Vaishnavi Ahuja EXTERNAL
- Varun Chaudhary EXTERNAL
- vedant paul EXTERNAL
- Vihan Singhai EXTERNAL
- Vivekanand Tiwari EXTERNAL
- Yash Dayal EXTERNAL

Re: Invitation for lecture from Industry person - Reg

Nalla Dhanunjay <dhanunjaynalla@gmail.com>

Sat 10/24/2020 2:02 PM

To: Vikram Kulkarni (Dr.) <Vikram.Kulkarni@nmims.edu>

Cc: Ketan Shah (MPSTME - Mumbai) <KetanShah@nmims.edu>; Bhisaji Surve <Bhisaji.Surve@nmims.edu>; anishkamoona@gmail.com <anishkamoona@gmail.com>; atreyaagastya@gmail.com <atreyaagastya@gmail.com>

📎 1 attachments (242 KB)

Life cycle of an Embedded IC.pdf;

Dear Vikram Sir,

Thank you very much for arranging the session.

Please find the presentation attached herewith and please do not hesitate to reach me for any clarification/questions.

Wish you a great week ahead and Happy festival season.

Thanks & Regards,

Dhanunjay Nalla

On Fri, 23 Oct 2020 at 16:53, Vikram Kulkarni (Dr.) <Vikram.Kulkarni@nmims.edu> wrote:

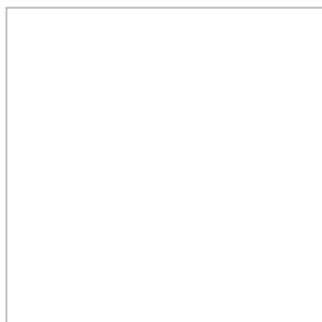
Dear Mr. Dhanunjay,
[Semtech Neuchatel, Switzerland.](#)

I heartily welcome you to deliver the lecture on "Embedded systems" tomorrow i.e, 24-10-2020 between **1pm to 2pm** Indian Standard Time.

You can join the lecture with the following MS-Teams code or code

Team code: **qipw3dh**

<https://teams.microsoft.com/j/team/19%3a6cf40683deb9448e992dff1f9ebbf4a8%40thread.tacv2/conversat...>



Join conversation

teams.microsoft.com

Short Profile of Mr. Dhanunjay,

Dhanunjay Nalla received his [B.Tech degree](#) in Electrical and Electronics Engineering from **Jawaharlal Nehru Technological University** and [M.Tech degree](#) in Electrical Engineering from **IIT Kharagpur** in 2010 and 2012 respectively.

He is currently working for Semtech Neuchatel, Switzerland as a Staff Test Engineer.

Prior to this role he worked for **Advantest SAS, Grenoble France** as an Application Engineer from 2016 to 2019 and at **Cypress Semiconductors pvt. Ltd., Bangalore India** as a Senior Test Engineer from 2012 to 2016.

He is a co-author for,

1. "A Built in Self Test System for Dynamic Performance Parameter Evaluation of Pipelined Analog to Digital Converter", Proceedings of the World Congress on Engineering and Computer Science 2013 Vol II WCECS 2013, 23-25 October, 2013, San Francisco, USA.

2. "Pipelined Analog to Digital Converter and Fault Diagnosis", IOP Publishing Ltd 2020
ISBN: 978-0-7503-1730-6.

Thanking you.

Thanks and Regards

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Dhanunjay Nalla
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Recapitulation

- What is an IC?
 - Integrate several circuits on a single substrate
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 - Make the device ready to use. IC -> device -> FW -> OS -> Apps
- What is the importance of an Embedded IC?
 - Growing needs of the human being to become ...

Stages of IC life

- Concept
- Specifications
- Design & Layout
- Verification
- Tape out
- Fabrication
- Firmware
- Characterization and testing
- Qualification and Release
- Manufacturing

Stages of IC life

- **Concept**
- Specifications
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Concept

- Engage with the customer(s) to get their needs
 - Mobile carrier company needs a radio to support 5G standards
 - Other one is looking for a hexa-deca (16) core processor for next gen smartphone
 - Another one is looking for xyz ...
- Get fascinated to your specifications / design
- Marketing team will be more active at this stage
- Feedback to the design team from the customers
 - About the requirements from the customer
 - Specifications
- Keep track of the expected “future” demand from customer

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Specifications

- Design team gets an idea on the device specifications
- Decide to design new one or to reuse existing (with improvements)
- Assume, new design is needed
- Prepare floor plan
- Block level specifications.
 - Ex: Need a 16 - core processor to run at 4 GHz
 - 5G radio : support many bands, different speeds

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Design & Layout

- Synthesis the block level specifications into sub blocks / IP level
 - Ex: Need 16x1 / 8x2 / 4x4 IPs for a 16-core processor
- Assume, you need to use 16 x 1-core IP.
- Design 1-core IP that can run at 4 GHz.
- Interconnect all cores to get to the necessary block
- When the transistor level design is ready, prepare the layout
- Run the simulations again on the layout.

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Verification

- Verify the design is functioning as per the expectations & matching the specifications
- Simulations on the design level
- Use test benches to model the blocks (in addition to the actual design)
- Feedback the results to the design until expected block is ready
- Could use FPGA to mimic the device

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Tape out

- Once the design is ready, all simulations are ready, verification is complete
- Send the layout metal masks & die floor plan, foot prints etc to foundry
- Prepare:
 - HW for test, reliability, characterization
 - Test / characterization program
 - FW
 - Validation -> test cases for FW
 - Customer code
- Get ready for wafer / packages.

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Fabrication

- Wait for the foundry to deliver the wafers together with the wafer attribute data
- WAT data is very important to identify the device behaviour before testing
- Fab-deviations, process variations are caught by WAT.

Stages of IC life

- Concept
- Specifications
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- **Firmware**
- Characterization and testing
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Firmware

- IC is getting ready, what is next?
- How do you verify / test / use the bare IC?
- Prepare the FW before the devices arrives
- The software that controls the device functionality
- Two types:
 - Permanent FW: store in ROM, load before tapeout.
 - One time yet lot of effort
 - Flexible FW: Store in Flash, load anytime, as many times as you want
 - Need to integrate Flash, one time investment, reap the fruits forever
 - Often is used to re/cover the design issues

Firmware

- Language: ASM, C, few other
- Requirements: Minimum, efficient, real time, stable, easy to read ...
- Errors: are very expensive
 - A good FW can make bring life to a scrap device
 - A very small error can turn \$tn product into scrap
- Minimize processor activity, ex: battery powered devices

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Characterization & Testing

- Wafers are ready, if needed, assemble the devices into the packages.
- For wafer test, need to be ready with the Test/Characterization programs.
- Bulk testing - ATE is needed.
- Characterization – Bench setup (DPS, VI, OSC, AWG, ...) / ATE
- Need to have the proper hard ware (PCB, sockets, Probe card etc) before starting test / char
- On ATE, need to have the test program
- Char – Sweep the device behaviour across PVT corners to find the pass-fail boundary and values for all specifications at this boundary
- Device is meeting all specifications → proceed for bulk testing
 - If not, go back to design and repeat

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Qualification & Release

- Bulk Testing:
 - Prepare and debug the production test program – must be on an ATE
 - Test wafers (6", 8", 10", 12") / Packages (DIP, QFN, SOIC, BGA, WLCSP, ...)
- Reliability Tests:
 - Make sure device life time is as per the design expectations
 - Perform stress tests, to avoid field failures
- Once devices pass through Reliability test, freeze the test program and submit for the Test houses (in-house testing or OSATs)
- Six Sigma, Gaussian distribution
- Statistical Analysis of test results

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Manufacturing

- Once the device pass all Reliability tests, it is the time to sell
- Fab will produce the wafers
- Test house performs testing WT or FT
- Operation team will take care of the post release activities.
- Sell to customers : direct or distributor
- Zero inventory:
 - Take orders with a lead time
 - Fabricate, Test & Sell within the lead time
 - No extra expenses in maintaining the inventory
 - No available finished good in the inventory
 - Need to have the fab, test, assembly houses available all the time

How this could help you?

Role	Requirements
Program Manager	Business administration with strong electronic background
Design Engineer	Design & layout, must have deep understanding of transistor level circuits
Verification Engineer	Verification, Deep understanding of transistor level together with HDLs
Product Engineer	Thorough understanding of processes from transistor level to package part
Test / Characterization Engineer	Thorough understanding of transistor level circuits, ATE knowledge & HL languages
System Engineer	Knowledge of HDL, block level understanding of circuits
Software / FW Engineer	Register level understanding of a circuit & low level languages
Validation Engineer	Block level understanding & high level languages
(Field) Application Engineer	Block level understanding & low level + high level languages, 20% travelling
Marketing	Business administration with Electronic background
Failure Analysis Engineer	Block level & register level understanding, FA instruments
Other cross functional roles	To facilitate all the above roles to ease the execution of their job

Questions?